**IN THE SPECIFICATION:**

Please amend page 18, line 9, to page 19, line 8, as follows:

In FIG. 4, first, the synchronization control circuit 40 supplies a synchronization command signal G1 in logic level 1 to the timing generation circuit 50 (step S40). By executing the step S40, the counter 503 of the timing generation circuit 50 takes in a predetermined counter initial value each time a synchronization detection signal SYC in logic level 1 is supplied, thus making a count-up operation. Due to this, from the decoder 505 is outputted a data fixing signal FX, address demodulated timing signal AX and synchronization demodulation timing signal SX as noted before in timing synchronization with the synchronization detection signal SYC. After executing the step S40, the synchronization control circuit 40 supplies the address counter 41 with an address normal-state signal G2 in logic level 0 representative of not having acquired a normal address (step S41). By executing the step S41, the counter ~~41 of the timing generation circuit 50~~ 411 of the address counter 41 operates by itself. Next, the synchronization control circuit 40 determines whether or not the synchronism-abnormality detection signal AB is in level 1 representative of a synchronism abnormality (step S42). While, in the step S42, the synchronism-abnormality detection signal AB is in logic level 1, i.e. if determined that a synchronization signal could not have been read from the recording disk 30, the synchronization control circuit 40 returns to the step S40 and repetitively executes the foregoing operation.

Please amend page 19, line 9, to page 20, line 9, as follows:

Meanwhile, in the case, in the step S42, the synchronism-abnormality detection signal AB is not in logic level 1, i.e. in the case it is determined that a synchronization signal could have been correctly read from the

recording disk 30, the synchronization control circuit 40 supplies a synchronization command signal G1 in logic level 0 to the timing-signal generation circuit 50 (step S43). By executing the step S43, the counter 503 of the timing generation circuit 50 operates by itself. Next, the synchronization control circuit 40 determines whether or not an error zero signal E0 is in logic level 1 representative of a state free of error (step S44). In the step S44, when it is determined that the error zero signal E0 is not in logic level 1, i.e. an error exist in the address data AD, the synchronization control circuit 40 supplies the address counter 41 with an address normal-state signal G2 in logic level 0 representative of not having acquired a normal address (step S45). By executing the step S45, the counter ~~41 of the timing generation circuit 50~~ 411 of the address counter 41 operates by itself. Next, the synchronization control circuit 40 determines whether or not the address continuous changes signal AN represents an address continuous changes greater than a predetermined number P (step S46). If it is determined in step S46 that the address continuous changes signal AN is not greater than the predetermined number P, the synchronization control circuit 40 returns to the step S42 and repetitively executes the foregoing operation.

Please amend page 23, line 8, to page 24, line 15, as follows:

In the address normal state ST2, an address normal state signal G2 in logic level 1 is supplied to the address counter 41 (step S47). Due to this, the address counter 41 takes in the corrected address data ADR and increases (or decreases) the address data value thereof by 1 at one time, thereby creating generated address data ADC and supplying it to the recording/reproducing control circuit 42. If the corrected address data ADR is determined having an error ~~(E0="1")~~ (E0="0") and the corrected address data ADR is determined having continuously changed a number of

times greater than the predetermined number P, an address normal state signal G2 in logic level 0 is supplied to increase (or decrease) by 1 at one time the value of address data acquired before. In this duration, the address normal state ST2 is maintained unless the address data AD read out from the recording disk 30 and demodulated is determined to be uncorrectable consecutively a number of times greater than a predetermined number of times Q (step S48). Meanwhile, in the case that the address data AD is determined to be uncorrectable consecutively a number of times greater than the predetermined number of times Q, i.e. in the case the corrected address data ADR is determined an incorrect address, the process returns to a synchronization state ST1. Namely, in the case that the corrected address data ADR is determined as not a correct address, it is determined that there is a possibility of going out of synchronism under influence of a certain external disturbance, and the process returns to the synchronization state ST1 where determination is made for a synchronization state. As a result, in the case of a determination of going out of synchronism, a synchronization command signal in logic level 1 is sent to thereby effect a re-synchronism process (loading the counter 503 with an initial value in timing synchronization with the synchronization detection signal SYC).